CLAIMS

What is claimed is:

1. A method for generating a random bit stream comprising:
   accumulating a plurality of hardware driven numbers;
   extracting a portion of each hardware driven number; and
   combining each extracted portion to form a random bit stream.

2. The method of Claim 1 wherein accumulating a plurality of hardware driven numbers comprises:
   reading a timestamp; and
   storing the timestamp.

3. The method of Claim 2 wherein extracting a portion of each hardware driven number comprises extracting one or more lower order bits from each hardware driven number.

4. The method of Claim 1 wherein accumulating a plurality of hardware driven numbers comprises:
   determining the quantity of hardware driven numbers required to achieve a pre-established output bit rate using a predefined de-skewing mechanism; and
   accumulating the determined quantity of hardware driven numbers.

5. The method of Claim 1 wherein extracting a portion of each hardware driven number comprises extracting one or more bits from each number.

6. The method of Claim 1 wherein combining each extracted portion comprises:
   concatenating bits extracted from each number at a particular bit position; and
   de-skewing the concatenated result in order to provide a uniform distribution of random bits.

7. An apparatus for generating a random bit stream comprising:
   number receiver that receives hardware driven numbers;
   extractor that extracts a portion of a hardware driven number; and

bit stream generator that generates a bit stream according to a plurality of extracted portions of hardware driven numbers.

8. The apparatus of Claim 7 wherein the number receiver comprises:
time interface that is capable of receiving a timestamp; and
buffer that stores the timestamp.

9. The apparatus of Claim 8 wherein the extractor comprises a selection matrix that selects one or more of the least significant bits in the timestamp.

10. The apparatus of Claim 7 further comprises a cycle generator that comprises:
time base generator that generates a time base;
translation table that generates a de-skewing factor according to a bit rate indicator; and
count down divider that generates a number pulse by dividing the time base according to the de-skewing factor and wherein the translation table is populated with empirical data that correlates the efficiency of a de-skewing mechanism associated with the de-skewing factor and the bit rate indicator.

11. The apparatus of Claim 7 wherein the extractor comprises:
one or more input ports, each for receiving a data bit;
one or more output ports, each for driving a data bit; and
cross-bar switch for connecting a data bit from an input port to at least one output port.

12. The apparatus of Claim 7 wherein the bit stream generator comprises:
plurality of registers that accept extracted portions of hardware driven numbers and present a bit-wise concatenated result;
transition mapping table populated with de-skewing values that generates a de-skewed random number according to the concatenated result; and
shift register that serializes the de-skewed random number.

13. A random bit stream generator comprising:
processor capable of executing instructions;

memory; and

instruction sequences stored in the memory comprising:

number receiver module that, when executed by the processor, minimally causes the processor to retrieve a hardware driven number;

extractor module that, when executed by the processor, minimally causes the processor to extract a portion of a hardware driven number; and

concatenator module that, when executed by the processor, minimally causes the processor to generate a concatenated value by combining a plurality of extracted portions of hardware driven numbers in a bit-wise manner.

14. The random bit stream generator of Claim 13 further comprising a serializing output register capable of generating a serial bit stream according to at least one of the concatenated value and a de-skewed concatenated value.

15. The random bit stream generator of Claim 13 further comprising a hardware number generator capable of generating a timestamp and wherein the number receiver module minimally causes the processor to:

retrieve a timestamp from the hardware number generator; and

store the timestamp in a buffer region in the memory.

16. The random bit stream generator of Claim 15 wherein the extractor module minimally causes the processor extract a portion of a hardware driven number by extracting one or more lower order bits from a hardware driven number.

17. The random bit stream generator of Claim 13 further comprising a number pulse generator that is capable of issuing a number pulse signal to the processor and wherein the number receiver module minimally causes the processor to retrieve a hardware number from a hardware number generator according to the number pulse signal and wherein the period of the number pulse signal is selected according to a pre-established output bit rate using a predefined de-skewing mechanism.

18. The random bit stream generator of Claim 13 wherein the extractor module minimally causes the processor to extract a portion of a hardware driven number by minimally causing the processor to extract one or more bits from the hardware driven number.

19. The random bit stream generator of Claim 13 further comprising a de-skewing module instruction sequence stored in the memory that, when executed by the processor, minimally causes the processor to de-skew the concatenated value.

20. A computer-readable medium having computer-executable functions for generating a random bit stream comprising:

number receiver instruction sequence that, when executed by a processor, minimally causes the processor to accumulate a plurality of hardware driven numbers;

extractor instruction sequence that, when executed by a processor, minimally causes the processor to extract a portion of each hardware driven number; and

concatenator instruction sequence that, when executed by a processor, minimally causes the processor to concatenate a plurality of extracted portions of hardware driven numbers into a concatenated value in a bit-wise manner.

21. The computer-readable medium of Claim 20 wherein the number receiver instruction sequence minimally causes the processor to accumulate a plurality of hardware driven numbers by minimally causing the processor to:

read a timestamp from a hardware driven number generator; and

store the timestamp in a memory.

22. The computer-readable medium of Claim 21 wherein the extractor instruction sequence minimally causes the processor to extract a portion of each hardware driven number by minimally causing the processor to extract one or more lower order bits from the timestamp.

23. The computer-readable medium of Claim 20 wherein the number receiver instruction sequence minimally causes the processor to accumulate a plurality of hardware driven numbers by minimally causing the processor to accumulate a quantity of hardware driven numbers over a period of time wherein the quantity of hardware driven numbers

accumulate over the period of time is selected according to a pre-established output bit rate and a predefined de-skewing mechanism.

24. The computer-readable medium of Claim 20 wherein the extractor instruction sequence minimally causes the processor to extract a portion of each hardware driven number by minimally causing the processor to extract one or more bits from each hardware driven number.

25. The computer-readable medium of Claim 20 further comprising a de-skewing instruction sequence that, when executed by a processor, minimally causes the processor to de-skew the concatenated value.

26. A random bit stream generator comprising:
means for accumulating a plurality of hardware driven numbers;
means for extracting a portion of each hardware driven number; and
means for combining each extracted portion to form a random bit stream.

27. The random bit stream generator of Claim 26 wherein the accumulating means comprises:
means for reading a timestamp; and
means for storing the timestamp.

28. The random bit stream generator of Claim 26 wherein the accumulating means comprises:
means for accumulating a selected quantity of hardware driven numbers over a period of time wherein the selected quantity is selected according to a pre-established output bit rate and a predefined de-skewing mechanism.

29. The random bit stream generator of Claim 26 wherein the extracting means comprises a means for extracting one or more bits from a hardware driven number.

30. The random bit stream generator of Claim 26 wherein the combining means comprises:
concatenating means for bit-wise concatenating the extracted portions into a concatenated value; and
de-skewing means for de-skewing the concatenated value in order to result in a uniform distribution of random bits.